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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/666,972	09/19/2003	Louis L. Hsu	728-203 DIV (YOR9-2001-01	8609

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EXAMINER	
IM, JUNGHWA M	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 03/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/666,972	HSU ET AL.	
	Examiner	Art Unit	
	Junghwa M. Im	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21,23-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21,23-34 and 38-40* is/are rejected.

7)☒ Claim(s) *35-37* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/23/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 21, 23-27, 29-30, 33-34 and 38-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agarwal et al. (US 5510630), hereinafter Agarwal in view of Nemati et al. (US 6229161), hereinafter Nemati and Krautschneider et al. (US 5821591), hereinafter Krautschneider.

Regarding claim 21, Figures 3A-3H of Agarwal show a method for fabricating a memory array having a plurality of memory cells, the method comprising the steps of:

providing a wafer having at least one silicon carbide (SiC) layer (col. 6, lines 45-49); and fabricating each of the plurality of memory cells [14 in 3H and col. 1 , lines 9-10]over the at least one SiC layer.

Agarwal shows the most aspects of the instant invention except that the memory cells are T-RAM memory cells. Nemati shows in Fig. 1 a memory device with a T-RAM. It would have been obvious to one of ordinary skill in the art at the time of the invention to have T-RAM memory cells of Nemati a memory array of Agarwal since such a memory device with a SRAM with a thyristor ensures a smaller size of a device and low power consumption (col. 1, lines 28-32). Alternatively, it would have been obvious to one of ordinary skill in the art at the time of

the invention to form the Nemati memory on SiC, as taught by Agarwal to achieve the advantages of SiC such as operation at high temperature due to high band gap.

The combined teachings of Agarwal and Nemati fail to show that "each of the plurality of memory cells includes a first and a second vertical device, said first and second vertical device being approximately the same height." Fig. 7 of Krautschneider shows a memory cell comprising a plurality of the vertical devices with the same height. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Krautschneider into the T-RAM memory cells of Agarwal and Nemati in order to have each of the plurality of memory cells including a first and a second vertical device, said first and second vertical device being approximately the same height for reduction of the device area.

Regarding claim 23, Krautschneider shows each of the plurality of memory cells has a size of less than of equal to $6F^2$ (Abstract).

Regarding claims 24 and 25, Nemati shows in Fig. 1, each of the plurality of T-RAM memory cells include a first and a second device, wherein the first device is a thyristor 10 and the second device is a transfer gate 20.

Regarding claim 26, Figure 3F of Agarwal shows further comprising the step of encapsulating each of the plurality of memory cells with an insulating material (44; col. 9, line 5).

Regarding claim 27, Figure 3F of Agarwal shows further comprising the step of fabricating each of the plurality of memory cells with a planar cell structure (col. 9, lines 17-18).

Regarding claims 29 and 30, Nemati shows in Fig. 6a (and col. 5, line 62 – col. 6, line 5) shows the method wherein the step of fabricating each of the plurality of memory cells on the wafer includes the steps of doping portions of the wafer with a first doping implant (p); and doping portions of the wafer in proximity to the portions doped with the first doping implant with a second doping implant (n).

Regarding claim 33, Agarwal discloses that the layer 24 is n-doped (col. 6, lines 49-50) and the layers 18 and 20 are epitaxially grown (col. 5, lines 21-25), and fails to show a method wherein "the wafer includes a first layer formed by implanting an. n+ type arsenic implant at an energy in the range of 2 to 15 KeV and a dosage of between 8E14/cm2 to 3E15/cm^2; a second layer formed by epitaxial growth using p-type boron at a dosage of between 4E13/cm^2 to IE14/cm^2; and a third layer formed by epitaxial growth using n- type arsenic at a dosage of between 2E13/cm2 to 8E13/cm^2." However, it would have been obvious to one of ordinary skill in the art at the time of the invention made to have a recited doping value for boron/arsenic, since it would have been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only in routine skill in the art. *In re Aller,* 105 USPQ 233.

Regarding claim 34, the combed teachings of Agarwal, Nemati and Krautschneider do not explicitly show the method further comprising the steps of "providing a first mask to conceal the portions of the wafer doped with the first and second doping implants; etching portions of a first layer of the wafer which are not concealed by the first mask; dielectric layer over the wafer; and providing a second mask and etching portions of a second layer of the wafer which are not concealed by the second mask." However, Agarwal discloses in Figures 3A-3B that a layer with

a specific conductivity is formed by a conventional/well-known method of masking and etching the layer (col. 6, line 61 – col. 7, line 5). Therefore, it would be obvious to form a layer shown in Fig. 6a of Nemati is formed by the steps of "providing a first mask to conceal the portions of the wafer doped with the first and second doping implants; etching portions of a first layer of the wafer which are not concealed by the first mask; dielectric layer over the wafer; and providing a second mask and etching portions of a second layer of the wafer which are not concealed by the second mask."

Regarding claim 38, Figure 3F of Agarwal shows the at least one SiC layer is a p-type layer (col. 3, line 52).

Regarding claim 39, it is obvious that each of the plurality of memory cells of Agarwal is operational at high temperatures and in high radiation prone environment since the device is fabricated over a silicon carbide which has a high thermal conductivity (col. 2, lines 21-29).

Regarding claim 40, it is obvious that each of the plurality of memory cells of Agarwal is configured for being operational in a temperature range from 200 to 100 degree Celsius since the device is fabricated over a silicon carbide which has a high thermal conductivity (col. 2, lines 21-29).

Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Agarwal, Nemati and Krautschneider in view of Weidenheimer et al. (US 6154477), hereinafter Weidenheimer.

Regarding claim 28, the combined teachings of Agarwal, Nemati and Krautschneider fail to show a method comprising the step of providing three layers on the wafer prior to the fabricating step, wherein a first layer is provided on top of the at least one SIC layer and is an

n-type layer, a second layer is provided on top of the first layer and is a p-type layer, and a third layer is provided on top of the second layer and is an n-type layer. Fig. 2 of Weidenheimer shows three-layered (n-p-n) structure fabricated on the p type SiC wafer (col. 5, lines 6-23).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Weidenheimer into a memory array of Agarwal, Nemati and Krautschneider in order to have n-p-n layered structure on top of the SiC layer to reduce the noise.

Claims 31 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agarwal, Nemati and Krautschneider as applied to claim 29 above, and further in view of Sneelal et al.(US 6391720), hereinafter Sneelal

Regarding claim 31, the combined teachings of Agarwal, Nemati and Krautschneider show the most aspect of the instant invention except a method of "the step of doping portions of the wafer with a first doping implant includes the step of using a p-type boron implant at an energy in the range of 0.5 to 2 KeV and a dosage of between 2E14/cm^2 and 8E14/cm^2 as the first doping implant." Sneelal discloses a method of implanting boron at an energy in the range of 0.5 to 2 KeV and a dosage of between 2E14/cm^2 and 8E14/cm^2 (col. 5, lines 14-15).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Sneelal to a memory cell of the device of Agarwal, Nemati and Krautschneider in order to have a first doping implant including the step of using a p-type boron implant at an energy in the range of 0.5 to 2 KeV and a dosage of between 2E14/cm^2 and 8E14/cm^2 to accommodate the design specification. In addition, it would have been obvious to

one of ordinary skill in the art at the time of the invention made to have a recited doping value for boron implant, since it would have been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only in routine skill in the art. *In re Aller,* 105 USPQ 233.

Regarding claim 32, the combined teachings of Agarwal, Nemati and Krautschneider show the most aspect of the instant invention except a method of "the step of doping portions of the wafer with a second doping implant includes the step of using an n-type arsenic implant at an energy in the range of 2 to 15 KeV and a dosage of between SE14/cm^2 and 3E15/cm^2 as the second doping implant." Sneelal discloses a method of implanting arsenic at an energy in the range of 2 to 15 KeV and a dosage of between SE14/cm^2 and 3E15/cm^2 (col. 5, lines 14-15).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Sneelal to a memory cell of the device of Agarwal, Nemati and Krautschneider in order to have a first doping implant including the step of using a p-type boron implant at an energy in the range of 2 to 15 KeV and a dosage of between SE14/cm^2 and 3E15/cm^2 to accommodate the design specification. In addition, it would have been obvious to one of ordinary skill in the art at the time of the invention made to have a recited doping value for boron implant, since it would have been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only in routine skill in the art. *In re Aller,* 105 USPQ 233.

Allowable Subject Matter

Claims 35-37 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments filed January 7, 2005 have been fully considered but they are not persuasive. The rejection stands, modified only to accommodate the amendments made to the claims by Applicant.

New rejections are made in response to Applicant amended claims and the language of the rejection has been modified to meet the amended claim limitations. In particular, Krautschneider is referred to meet the modified limitation of "each of the plurality of memory cells includes a first and a second vertical device, said first and second vertical device being approximately the same height" Figure 7 of Krautschneider shows this aspect.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jmi

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SPE TC 2800